In column 7, line 6, pleas lace the second occurrence of " with --[216]214--.

In the Claims:

Please add the following new claims.

Sub B'

18. A method, comprising:

powering up an integrated circuit;

loading a first data bit into a master latch during the powering up of the integrated circuit;

generating a second data bit from the first data bit;

latching the first data bit in the master latch after powering up the integrated circuit; and

loading the second data bit into a slave latch after powering up the integrated circuit.

19. The method of claim 18 wherein powering up the integrated circuit comprises powering up the integrated circuit in a test mode.

20. The method of claim 18 wherein generating the second data bit comprises generating the second data bit equal to the first data bit.

21. The method of claim 18 wherein generating the second data bit comprises generating the second data bit equal to the complement of the first data bit.

22. The method of claim 18 wherein generating the second data bit comprises generating the second data bit during and after the powering up of the integrated circuit.

Sub B2

23. The method of claim 18 wherein:

loading the first data bit into the master latch comprises generating a clock signal having a first clock state; and

latching the first data bit in the master latch and loading the second data bit into the slave latch comprise generating the clock signal having a second clock stage.

24. The method of claim 18 wherein:

loading the first data bit into the master latch comprises generating a clock signal inside the integrated circuit, the clock signal having a first clock state; and

latching the first data bit in the master latch and loading the second data bit into the slave latch comprise generating the clock signal having a second clock state.

25. A method, comprising:

generating a power-on reset signal having a first reset state during a power up of an integrated circuit;

generating the power-on reset signal having a second reset state after the power up of the integrated circuit;

loading a first data bit into a master latch in response to the power-on reset signal having the first state;

generating a second data bit from the first data bit;

storing the first data bit in the master latch in response to the power-on reset signal having the second state; and

loading the second data bit into a slave latch in response to the power-on reset signal having the second state.

26. The method of claim 25 wherein:

said generating the power-on reset signal having the first state comprises generating the power-on reset signal having the first state when an integrated-circuit supply voltage has a first level; and

generating the power-on reset signal having the second state comprises generating the power-on reset signal having the second state when the supply voltage has a second level.

27. The method of claim 25 wherein:

generating the power-on reset signal having the first state comprises generating the power-on reset signal having the first state during a power up of the integrated circuit in a test mode; and

generating the power-on reset signal having the second state comprises generating the power-on reset signal having the second state after the power up of the integrated circuit in the test mode.

28. The method of claim 25 wherein generating the second data bit comprises generating the second data bit in response to the power-on reset signal having either the first state or the second state.

29. The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating a test signal having a first test state.

30. The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating multiple test signals each having a first test state.

31. The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise:

generating a test signal having a test state; and

generating a clock signal having a clock state in response to the test signal having the test state.

32. The method of claim 25 wherein:

loading the first data bit into the master latch comprises generating a clock signal having a first clock state in response to the power-on reset signal having the first reset state; and

storing the first data bit in the master latch and loading the second data bit into the slave latch comprise,

generating a test signal having a test state, and

generating the clock signal having a second clock state in response to the test signal having the test state.

33. The method of claim 25 wherein:

loading the first data bit into the master latch comprises,

generating a clock signal having a first clock state in response to the power-on reset signal having the first reset state,

generating a test signal having a test state, and

generating the first data bit in response to the test signal; and

storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating the clock signal having a second clock state in response to the power-on reset signal having the second reset state and the test signal having the test state.

34. The method of claim 25 wherein:

loading the first data bit into the master latch comprises,

generating a clock signal having a first clock state in response to the power-on reset signal having the first reset state,

generating a test signal having a first test state, and

generating the first data bit in response to the test signal; and

storing the first data bit in the master latch and loading the second data bit into the slave latch comprise,

generating the test signal having a second test state, and

generating the clock signal having a second clock state in response to the power-on reset signal having the second reset state and the test signal having the second test state.

35. A method, comprising:

powering up an integrated circuit;

loading a first data bit into a master latch during the powering up of the integrated circuit;

latching the first data bit in the master latch after powering up the integrated circuit; and

loading the first data bit into a slave latch after powering up the integrated circuit.

36. The method of claim 35 wherein:

loading the first data bit into the master latch comprises generating a clock signal having a first clock state; and

latching the first data bit in the master latch and loading the first data bit into the slave latch comprise generating the clock signal having a second clock stage.

37. The method of claim 35 wherein:

loading the first data bit into the master latch comprises generating a clock signal inside the integrated circuit, the clock signal having a first clock state; and